ALICE & BOB'S QUANTUM COMPUTING ROADMAP

The Path to the First Useful Quantum Computer

We cannot stress enough that a quantum computer which decoheres is not a quantum computer.

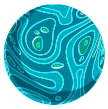
From our first steps in 2020, marked by our founders' paper in Nature Physics, to the release of our record-breaking Boson 4 chip on the cloud in May 2024, fighting decoherence has been our core mission. Today, after four years of continuous research, our cat qubit holds the world record among superconducting qubits for bit-flip times, and we're developing our first logical qubit.

Looking ahead, we're committed to launching Graphene in 2030, just one decade after we started. This will be a universal, fault-tolerant quantum computer designed to solve real-world problems. Although we've set milestones along the way, we've deliberately not set dates for these since the timing of research is rarely predictable. We liken this to playing golf: at the end of the round, we won't care if we met our predictions for each hole, but we'll care about wearing a green championship jacket in six years.

To achieve this, our five milestones, each tested and demonstrated on a distinct chip series, will move us closer to a practical quantum computer:

1. Master the Cat Qubit
Our Boson series will establish a reliable, reproducible cat qubit capable of storing quantum information and resisting bit-flip errors.

2. Build a Logical Qubit
Our Helium series will feature our first error-corrected, below-threshold logical qubit.



3. Fault-Tolerant Quantum Computing
Our Lithium series will connect logical qubits and demonstrate the first error-corrected logical gate.

4. Universal Quantum Computing
Our Beryllium series will implement a universal set of logical gates, enabled by magic state factories and live error correction.

5. Useful Quantum Computing
Our Graphene series will feature 100 low-error logical qubits that can be integrated into industrial computing facilities.

By 2030, we're confident that we'll have a computer that users will want to buy. And it won't be because it's quantum, but because it'll give results that won't be achievable in any other way.

Graphene will be the first of tomorrow's useful quantum computers, not the last. Its mission is to redefine the boundaries of computation. Our journey will continue, further scaling fault-tolerant quantum computers while further reducing errors.

Now, let's unfold our detailed research plan for the next five years.

IN A NUTSHELL

Since our inception, our mission has been to fight decoherence and develop fault-tolerant quantum computers. Leveraging our cat qubit, our goal is to create a useful quantum computer with 100 high-fidelity logical qubits by 2030. This is set to be the world's first quantum computer with meaningful applications, ushering in the dawn of the quantum era.

DOWNLOAD SHORT VERSION

// MILESTONE 1

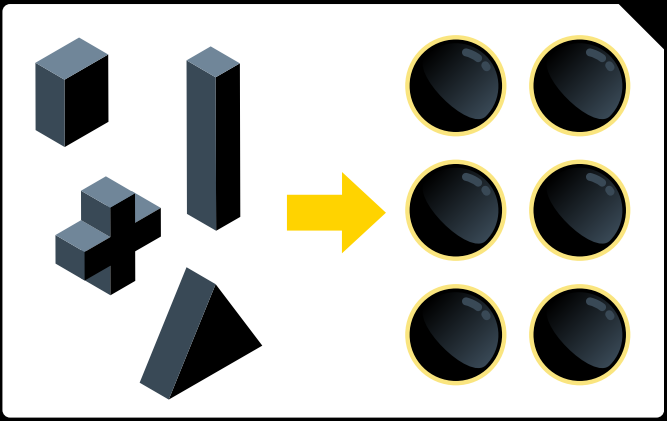
MASTER THE CAT QUBIT

2024 COMPLETE

During the 2010s, cat qubits were experimentally realized only a handful of times, and they didn't demonstrate their bit-flip protection qualities. The first cat qubit with its signature noise-bias wasn't successfully created and controlled until 2020. This seminal work by our founders, published in Nature Physics[1], led to the formation of Alice & Bob.

The first milestone of our journey was to master this new qubit, and we've done that. The release of Boson 4 on the cloud marked a foundational step toward building a quantum computer with cat qubits.

Challenge 1
Herd the Cats



In our formative years, each cat qubit was a unique experiment. We thought of them as handcrafted art pieces, each requiring specialized setups and adjustments. Unfortunately, their lack of reproducibility slowed our innovation.

To scale our quantum technology, we needed to master the reproduction and calibration of our qubits. Achieving this level of mastery demanded improvements in physics, hardware design, and nanofabrication.

By 2024, we had developed a deep understanding of these factors and adopted a standardized innovation process called DeepTech Motion.

Challenge 2
Achieve Record Bit-Flip Protection

Bit-flip protection is a cornerstone of our strategy. This allows cat qubits to efficiently run error correction at scale using far fewer qubits than other architectures. Over the years, our Boson series of single-cat chips has progressively raised the bar in bit-flip resistance and qubit design.

In 2023, our cat qubits were 10,000 times more resistant to bit-flip errors than our first-generation chips, achieving a bit-flip lifetime of 10 seconds. At the same time, we reduced cabling requirements and halved the overall footprint.

The culmination of these efforts was Boson 4, which we launched globally over the cloud in May 2024. This chip set the bit-flip lifetime record for any superconducting qubit: over 7 minutes. This achievement provided definitive proof that our cat qubits operate as theory predicts. We demonstrated that their intrinsic noise-bias makes them ideal for large-scale, hardware-efficient error correction.

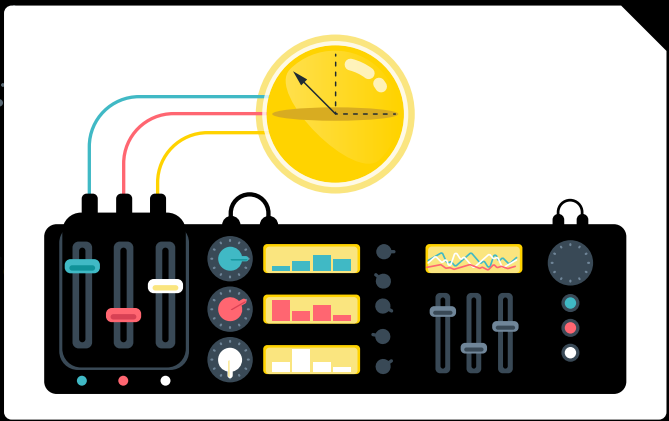
[1] Lescanne, R., M. Villiers, T. Peronnin, et al. "Exponential Suppression of Bit-Flips in a Qubit Encoded in an Oscillator." Nature Physics 16 (2020): 509–513. https://doi.org/10.1038/s41567-020-0824-x.

// MILESTONE 1

MASTER THE CAT QUBIT

2024 COMPLETE

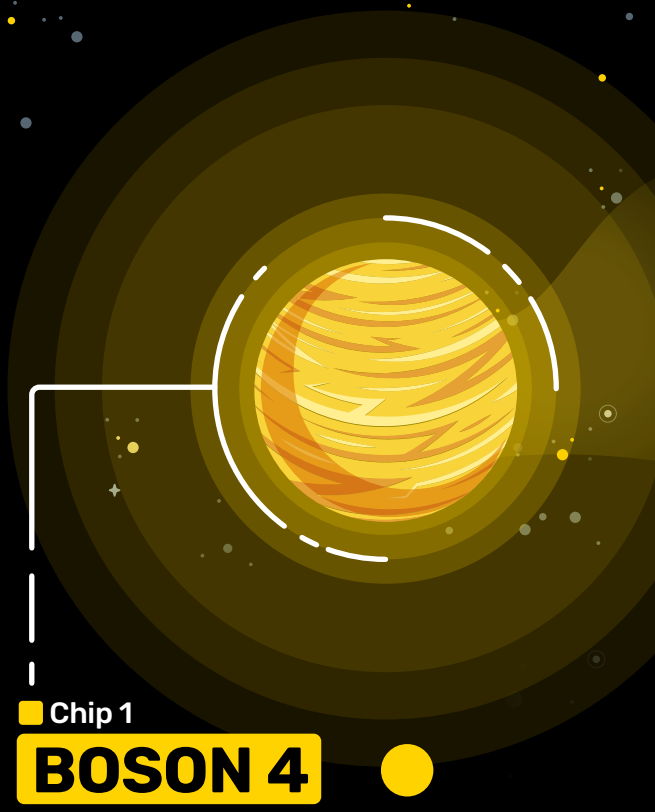
Challenge 3
Run Cat Qubit Operations



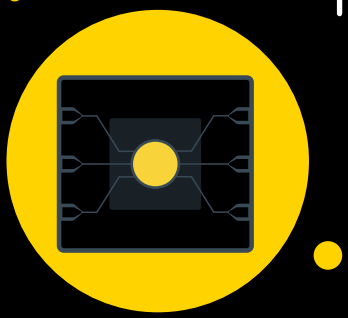
A single cat qubit, in isolation, can store a single quantum bit of information. To make meaningful use of this information, we need a suite of operations that can manipulate the qubit effectively.

The first critical step was developing elementary single-qubit operations: various state preparations, bit and phase measurements, and fundamental gates like the Z gate (phase gate). These operations aren't sufficient for running full quantum algorithms, but they lay the groundwork for a future universal gate set.

Our objective at this stage was to perform and validate these fundamental manipulations while preserving the cat qubit's inherent noise bias.



Chip 1
BOSON 4



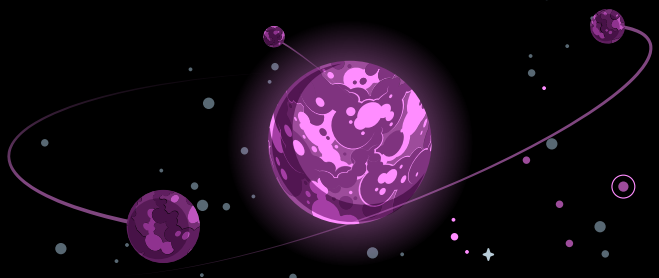
Cat Qubits 1

Logical Qubits 0

// MILESTONE 2

BUILD A LOGICAL QUBIT

WE ARE **HERE**

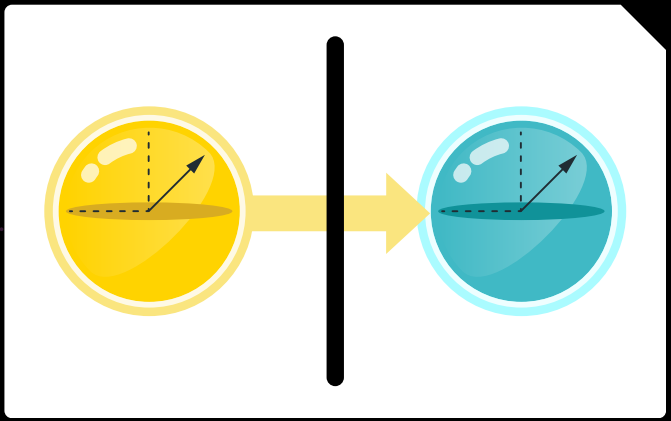


Now that we've mastered a single physical cat qubit, our next critical step is to develop a logical qubit. It must be error-corrected and under threshold. This is where we currently are on our roadmap, making this our primary goal at this time.

If you think about it, we protected our cats against bit-flip errors to reach our first milestone, so we're simply shifting our focus to the remaining error. This means adding a robust error correction process, which involves detecting and correcting phase-flips across a series of cats.

This milestone is necessary for building a fault-tolerant system. It will take us from developing a bias-preserving CNOT gate, through reliably detecting phase-flips, to connecting qubits in lines.

Challenge 1
Mirror the Phase

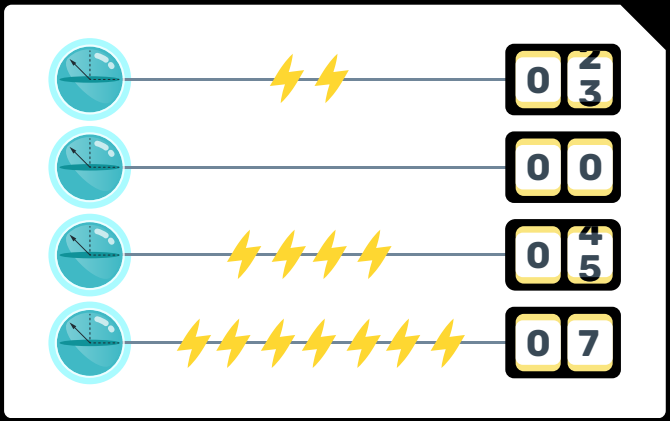


The first step in building a logical, error-corrected qubit is developing the Controlled-NOT gate, often referred to simply as the CNOT. The CNOT is a critical two-qubit operation that can 'mirror' the phase of one cat qubit onto another.

The importance of the CNOT is that it allows us to transfer the phase-flip effects affecting our data qubits to our auxiliary qubits. We can then measure the phases of the auxiliary qubits without corrupting the quantum information carried in the data qubits. The key challenge here is that our CNOT gate must be bias-preserving. In other words, it must not reintroduce bit-flip errors, as that would undermine the cat qubit's noise-bias advantage.

In March 2024, at the meeting of the American Physical Society, we presented promising experimental results from our Hydrogen chip: we showed the first CNOT operation involving two cat qubits. Since then, we have made further improvements to the gate's speed and reliability, which helps to reduce the likelihood of reintroducing bit-flips.

Challenge 2
Count the Flips



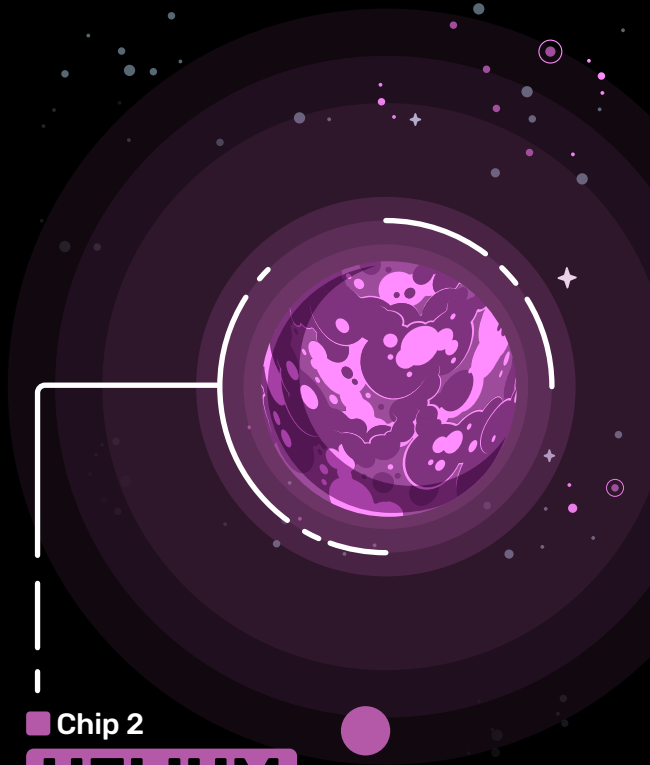
To detect and correct phase-flip errors, our next step will be to create a fast and reliable X measurement protocol. This measurement, also known as the phase measure or Mx, will allow us to interpret the results of CNOT operations. Specifically, we need to determine whether phase-flips have occurred and, if so, where.

The goal of the X measure is to repeatedly monitor the phases of the auxiliary qubits, which accumulate the results of multiple CNOT operations on the data qubits. For this mechanism to be useful on larger devices, such as our Helium chip series, it needs to be precise and fast.

// MILESTONE 2

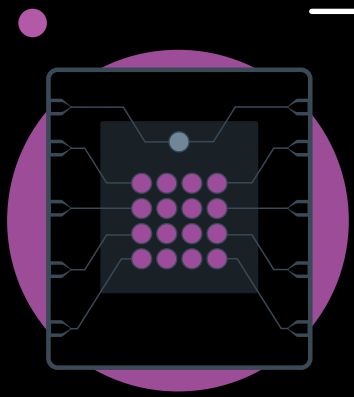
BUILD A LOGICAL QUBIT

WE ARE **HERE**



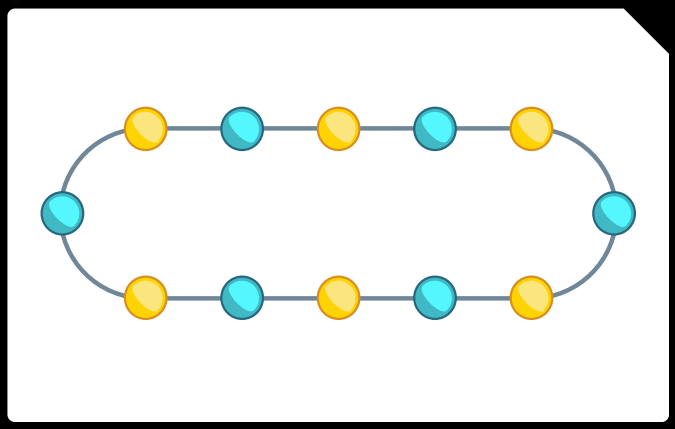
Chip 2

HELIUM



Cat Qubits	16
Logical Qubits	1
Clock Speed (μs)	1.5
Logical Error Rate	10^{-2}

Challenge 3
Link the Qubits



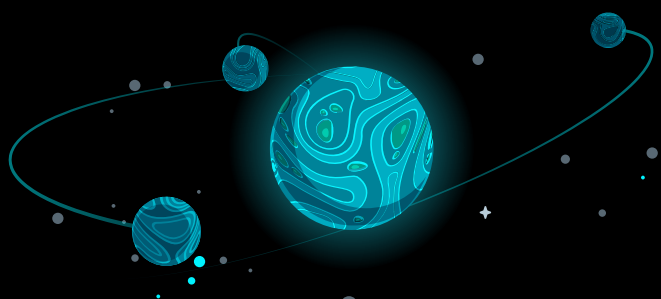
To fully implement quantum error correction, we need to run CNOT gates and phase measurements sequentially across multiple qubits in a chain. This is the cat qubit's signature error correction scheme, the repetition code. This crucial step requires degree-2 connectivity, meaning that each cat qubit must connect to at least two neighbors in a line.

As we create this linear arrangement of cat qubits, we need to ensure that their key features, such as their bit-flip protection and gate efficiency, don't degrade. Each additional connection brings a risk of introducing new noise or increasing errors, which would undermine our main goal: correcting errors.

We'll thoroughly test all the elements necessary for this connectivity on our Hydrogen chip. After that, we'll be able to launch our first under-threshold logical qubit chip, Helium. Hydrogen is a transitional chip series between Boson and Helium, which is why it is not listed as a milestone chip series.

// MILESTONE 3

FAULT-TOLERANT QUANTUM COMPUTING

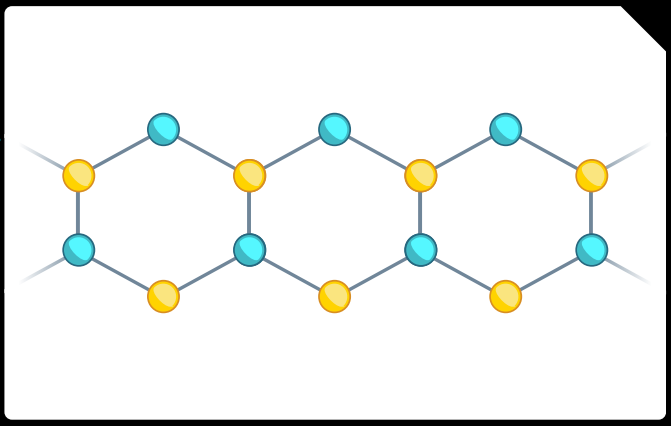


Once we have a single hardware-efficient logical qubit, our next major milestone will focus on scaling up our design to support a network of interacting logical qubits. This means moving to a robust, interconnected grid that enables logical quantum computations.

This third milestone will introduce a series of advances to support this scaling. These include establishing a hexagonal qubit grid and using advanced fabrication techniques to significantly increase qubit density. Equally important, we'll begin developing logical gates, with a focus on the logical CNOT gate as the foundation for universal quantum computing.

After these three challenges are cleared, we will tape out our first multi-logical qubit device, Lithium.

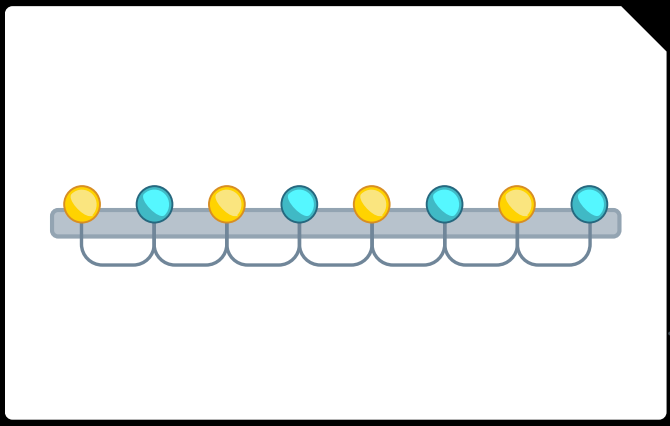
Challenge 1
Connect Logical Qubits



Creating a single, hardware-efficient logical qubit is an essential milestone, but useful quantum computers will require hundreds of interconnected logical qubits. To achieve this, we'll move from a linear, degree-2 connectivity to a complex, hexagonal, degree-3 grid structure. In this configuration, each physical cat qubit will be connected to three neighbors: two within their logical qubit and one from another logical qubit.

Establishing hexagonal connectivity introduces new engineering challenges, as these connections must not introduce additional noise or errors. Achieving this level of connectivity without performance degradation will be fundamental to building our Lithium chip, which will feature multiple logical qubits interacting with one another in a robust network.

Challenge 2
Double the Density



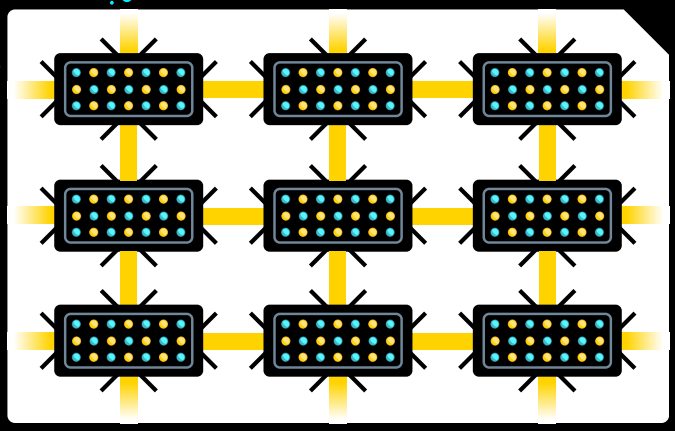
To scale quantum processors efficiently, we must fit significantly more cat qubits in a hexagonal grid layout onto a single chip. Increasing qubit density requires advanced fabrication techniques, notably flip-chip technology. This technology was developed for standard semiconductors but is now being applied to quantum devices as well.

This flip-chip approach allows circuits to utilize both sides of the processor, with qubits packed on one side and their connections printed on the other. This effectively doubles qubit density, while keeping the quantum processing unit's footprint unchanged.

// MILESTONE 3

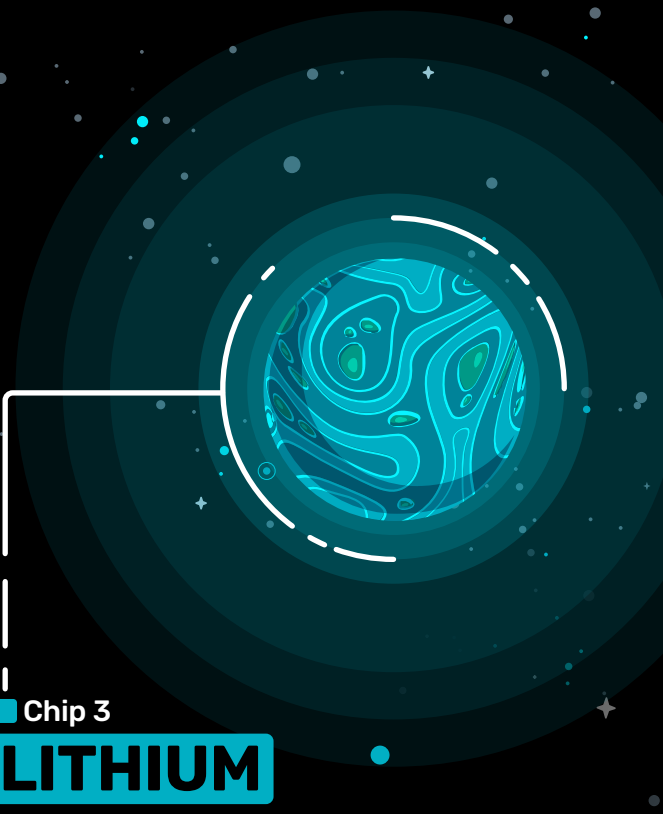
FAULT-TOLERANT QUANTUM COMPUTING

Challenge 3
Run a First Logical Gate

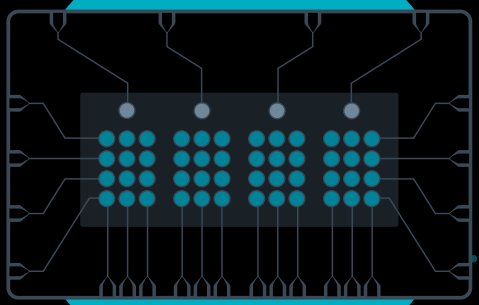


As we transition to working with logical qubits, it will become crucial to develop error-corrected logical gates. These gates must not reintroduce errors into already-corrected qubits. Developing a robust, logical CNOT gate, in particular, will be essential.

The logical CNOT serves as the cornerstone for fault-tolerant quantum operations. It is fundamental to multi-logical-qubit systems, like our upcoming Lithium chip, and will be the first logical gate in our universal gate set. This foundational set of gates forms the basis of all other gates and will enable us to perform universal quantum computations.



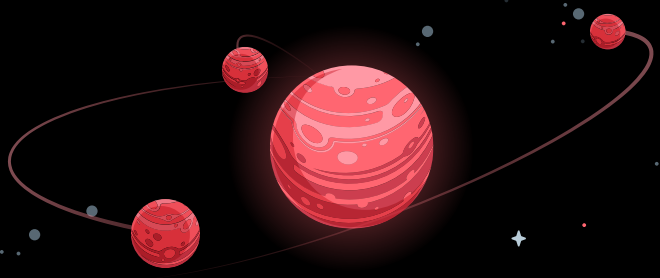
Chip 3
LITHIUM



Cat Qubits	48
Logical Qubits	4
Clock Speed (μs)	0.8
Logical Error Rate	10^{-3}

// MILESTONE 4

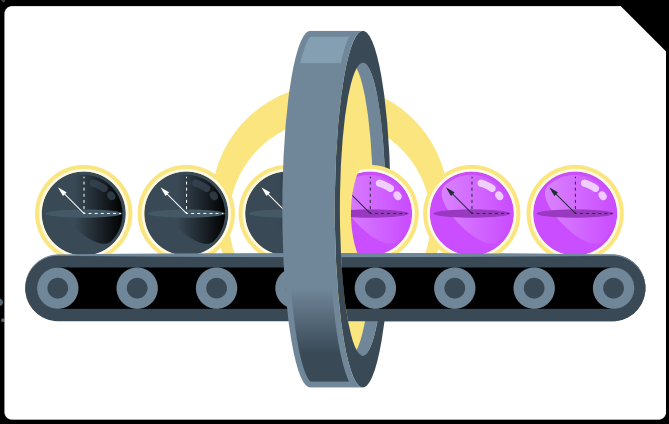
UNIVERSAL QUANTUM COMPUTING



A universal quantum computer is one that is capable of running any quantum algorithm, and a prerequisite for this is having a complete universal gate set. We must complete our set with the Toffoli gate, an advanced operation that requires solving two key challenges: producing a continuous stream of magic states and implementing live error correction. The latter monitors and corrects errors during gate operations. We will also develop our quantum firmware at this stage. The firmware will be a control layer essential for orchestrating the rapid hardware operations needed for our growing architecture.

With these advancements, the Beryllium chip series will be our first processors capable of universal quantum computing. They will lay the groundwork for larger systems designed to solve classically intractable problems.

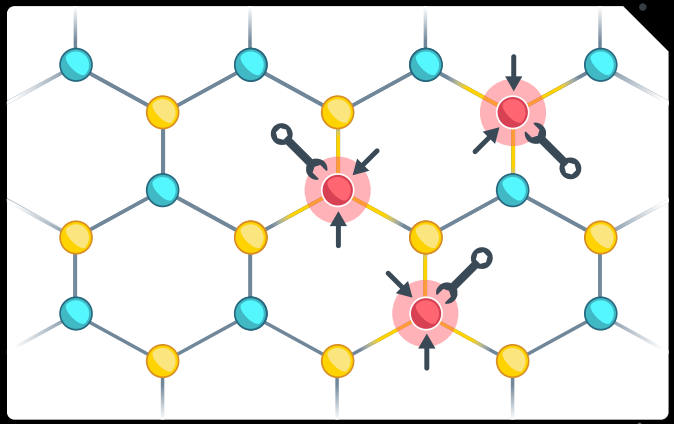
Challenge 1
Create Magic States



The Toffoli gate is a three-qubit gate that is critical for universal quantum computation. Implementing a logical Toffoli requires a continuous supply of qubits set in what is called a 'magic state.' These magic states get 'created' and 'spent' throughout an algorithm's execution. They are essential to maintaining the gate's logical integrity and preventing it from reintroducing errors into the system.

Creating a steady supply of these states, though, is both technically demanding and resource-intensive. It requires that we have specialized areas on our chip, which we designate as 'magic state factories.'

Challenge 2
Correct Errors, Live



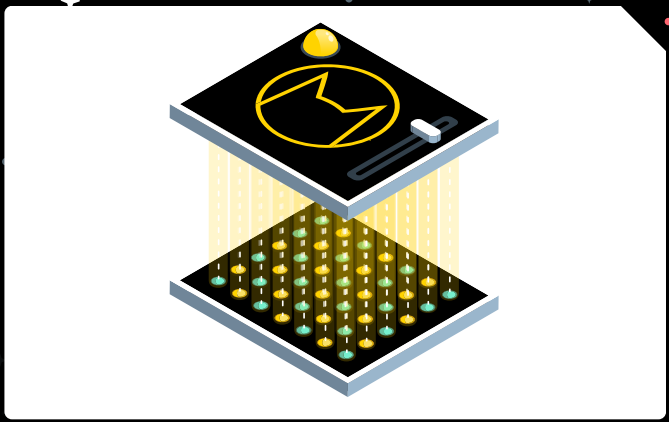
To implement gates like the Toffoli gate, our error correction process must be able to detect and address errors while our quantum algorithms are running.

To meet this challenge, we need to develop a fast and efficient 'live decoder.' This specialized classical computing functionality will allow us to correct errors rapidly enough to avoid slowing down operations. The live decoder must match the speed of the gate operations, ensuring that error correction remains synchronized with gate execution and doesn't introduce delays that could compromise the computation.

// MILESTONE 4

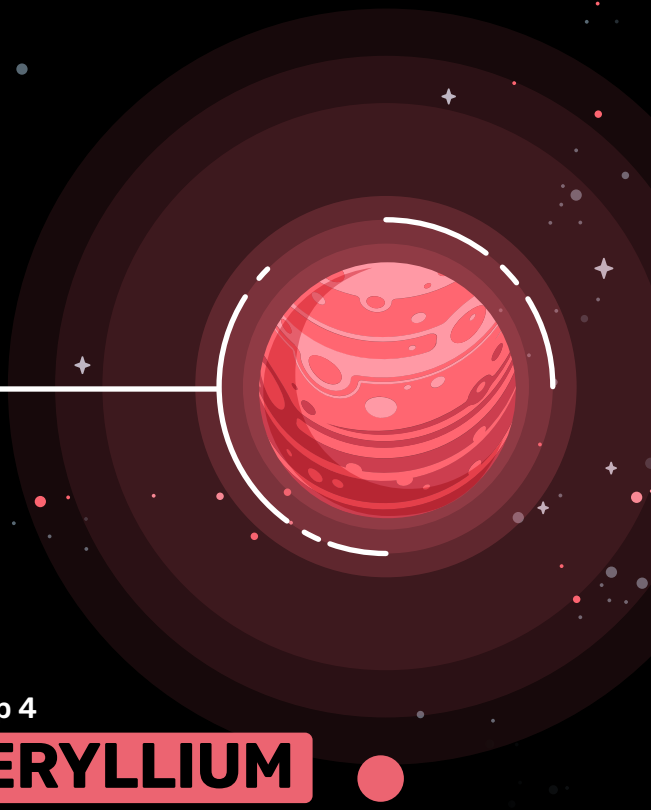
UNIVERSAL QUANTUM COMPUTING

Challenge 3
Build the Quantum Firmware

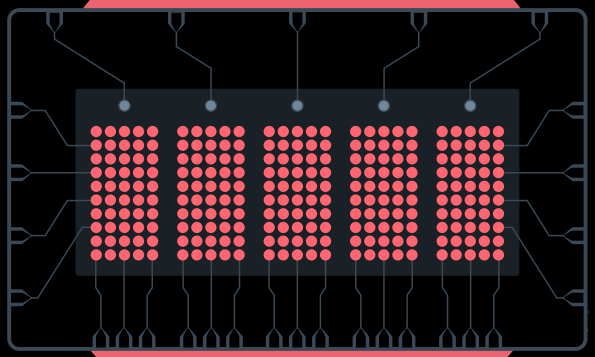


As our chips get larger and our gates grow in complexity, orchestrating the multitude of operations required at the hardware level becomes an increasingly formidable challenge. Each step in quantum computation depends on precise, synchronized pulses of microwave photons, which govern qubit behavior.

This is where the quantum firmware comes into play. You can think of it as a specialized operating system for our QPU. Firmware translates high-level algorithmic instructions into the exact control signals that each qubit responds to. This ensures that all operations are executed with the required timing and precision.



Chip 4
BERYLLIUM

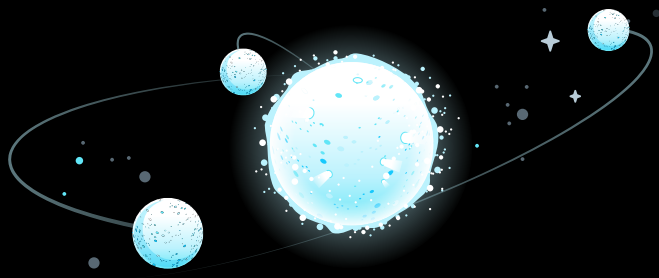


Cat Qubits	250
Logical Qubits	5
Clock Speed (μs)	0.8
Logical Error Rate	10^{-4}

// MILESTONE 5

USEFUL QUANTUM COMPUTING

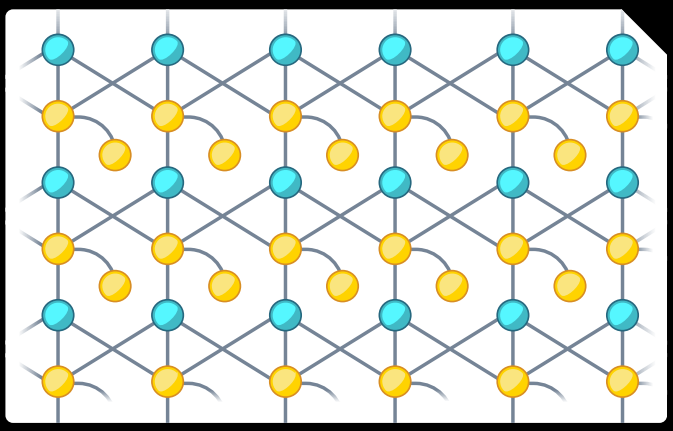
2030 START OF THE QUANTUM ERA



Estimates vary, but somewhere around 100 high-fidelity, logical qubits, we'll finally unlock some truly transformative applications for quantum computing. We'll be able to tackle problems that no classical computer can solve, delivering real-world value in fields like fundamental research. However, reaching this scale will require pushing hardware efficiency and quantum engineering to their limits.

In this phase, we will focus on maximizing the capability of every qubit and optimizing our hardware infrastructure. These engineering breakthroughs will form the foundation of our ultimate goal: building a universal, fault-tolerant quantum computer that demonstrates practical quantum advantage. It will be named Graphene, and we'll deliver it before the end of this decade.

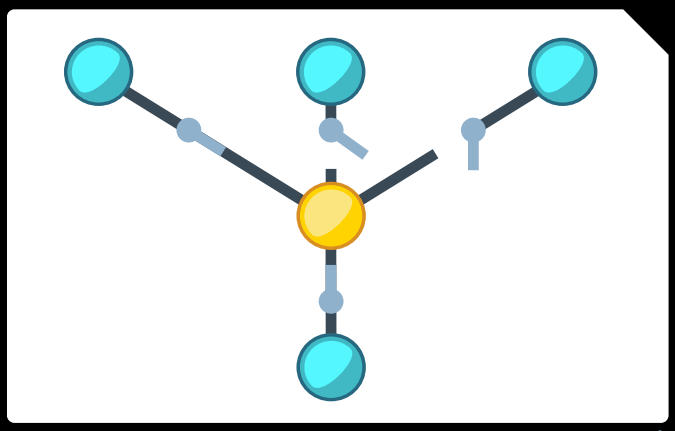
Challenge 1
Top-up Hardware Efficiency



Our goal is to reach the mathematical limits of hardware efficiency, and the connectivity degree required for LDPC (Low-Density Parity-Check) is key to achieving it. This advanced layout will connect each cat qubit with up to five neighbors, enabling reliable error correction with far fewer physical qubits than our already-efficient repetition code. Using Shor's algorithm as an example, we would need 3.5X fewer qubits, compared to our previous architecture, to factor a 2048-bit integer.

LDPC codes work by allowing physical qubits to contribute to more than one logical qubit simultaneously, thus, minimizing hardware use. This approach achieves comparable performance to other qubit technologies but, with cat qubits, uses up to 200 times fewer qubits[2].

Challenge 2
Switch Qubits



LDPC codes require selective connectivity, meaning specific qubits must interact under certain conditions with certain qubits without interfering with others. This is where tunable couplers come into play. Tunable couplers act as dynamic 'switches' that can connect and disconnect qubits on demand allowing intended interactions while preventing unwanted ones.

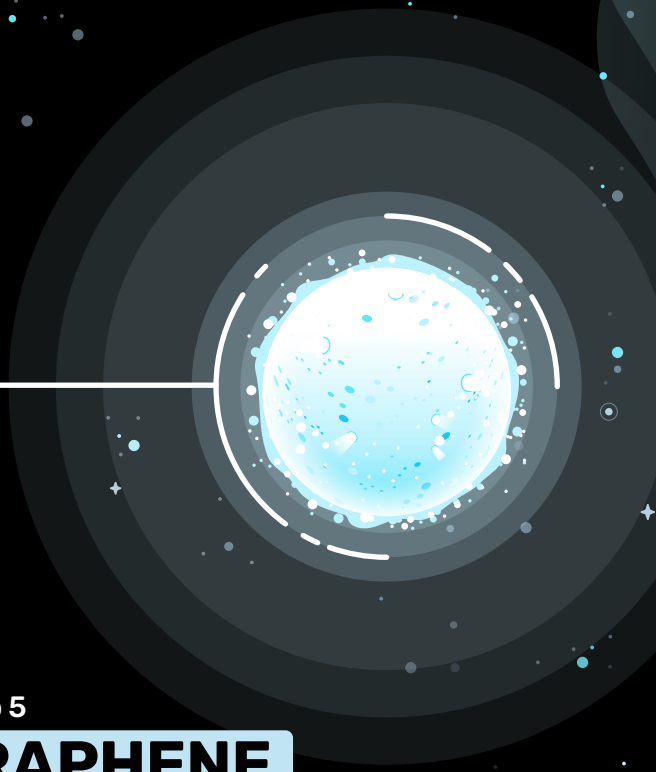
In our cat qubit architecture, tunable couplers must be developed with particular attention to preserving the qubits' inherent noise-bias properties. Additionally, by keeping qubit connections 'off' when their respective qubits aren't involved in a calculation, tunable couplers can reduce the potential for errors and optimize resource usage on the chip.

[2] Diego Ruiz, Jérémie Guillaud, Anthony Leverrier, Mazyar Mirrahimi, Christophe Vuillot. "LDPC-cat codes for low-overhead quantum computing in 2D" arXiv:2401.09541, https://arxiv.org/abs/2401.09541

// MILESTONE 5

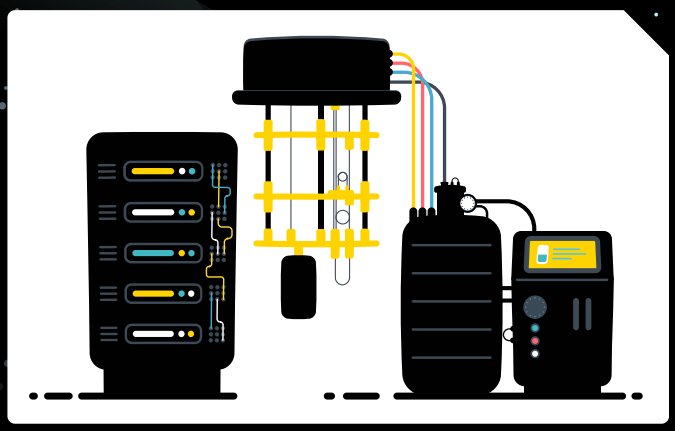
USEFUL QUANTUM COMPUTING

2030 START OF THE QUANTUM ERA



Challenge 3

Improve Enabling Technologies



As we produce larger quantum processors, the supporting infrastructure must evolve too. It must become far more efficient in terms of footprint, energy consumption, and operational complexity.

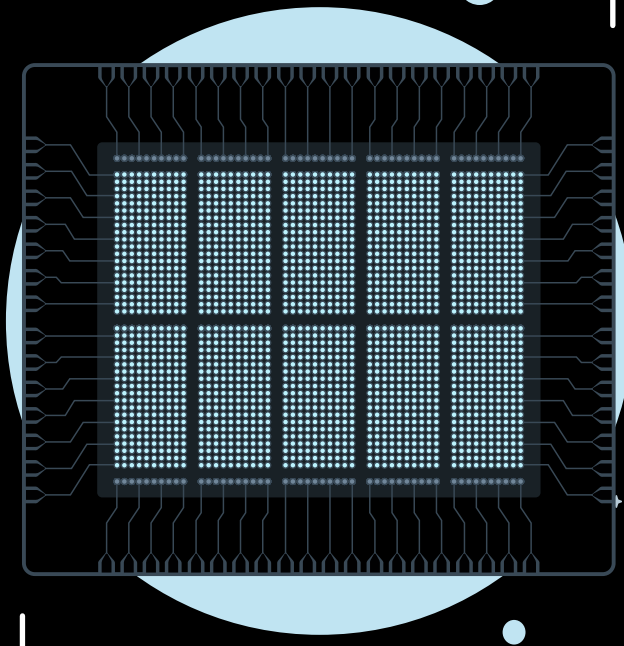
Quantum systems require incredibly complex environments to function: extensive cabling, electronics, classical computing resources for error correction, and fridges that reach temperatures colder than outer space. All of these resources scale with the number of qubits.

Luckily for us, cat qubits need far fewer physical qubits per logical qubit. This reduces the demand for infrastructure compared to traditional approaches.

Many industry players across the quantum hardware stack are actively contributing to this effort by scaling and refining cabling, microwave delivery systems, and cryogenic engineering. We will continue partnering with experts across these areas to integrate these enabling technologies into our first universal, fault-tolerant quantum computer. And by 2030, Graphene will be solving real-world use cases.

Chip 5

GRAPHENE



Cat Qubits	2000
Logical Qubits	100
Clock Speed (μs)	1
Logical Error Rate	10^{-6}

What's after that?

With 100 logical qubits, we will confidently step beyond classical computing's limits in simulating quantum reality. We'll escape both brute-force simulations and ad-hoc solutions, and with accuracy. Graphene will certainly thrill researchers in a variety of fields, but this accuracy will also allow us to solve problems with commercial value. This is the critical distinction between 100 logical qubits and 100 physical qubits.

Graphene will prove the feasibility of cat qubits as the preferred hardware for building universal fault-tolerant quantum computers. We will use our knowledge to continue building bigger and better quantum computers.

These next-generation devices will feature more logical qubits, lower error rates, and faster speeds, unlocking new applications for quantum computers. We'll have already provided a powerful new tool for fundamental science, material science, and chemistry, and we'll be looking toward applications in optimization and machine learning. We'll be opening up use cases in financial services, supply chain operations, and more. ■

Conclusion:

WHY DO WE DO ALL OF THIS?

WE'RE DOING WHAT WE'VE ALL BEEN TRAINED TO DO AS SCIENTISTS AND ENGINEERS: WE'RE CREATING SCIENCE APPLICATIONS.

HOWEVER, THAT'S JUST NOT THE CASE.

We're driven to build a useful quantum computer because the world needs to solve problems that are fundamentally beyond the reach of the most powerful classical computers we can build.

We live in a world where existential challenges demand ambitious technological solutions. What will be the role of humans in a future where another form of intelligence exists? How can we push the boundaries of drug discovery to combat disease? How can we fix the damage our society is causing to the ecosystem? How can we mitigate the risk of pandemics in an ever more interconnected and globalized world?

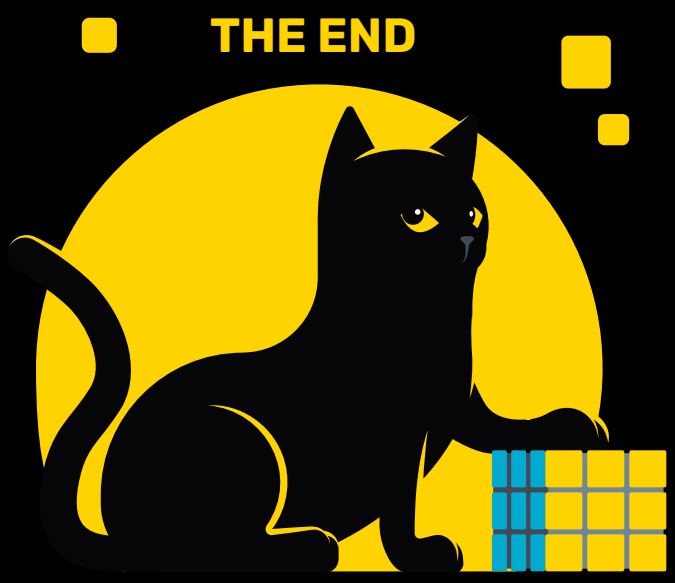
These are just a few examples. As engineers, physicists, and technologists, our contribution toward solving these questions is the responsible advancement of science and technology.

We're building a quantum computer for the countless curious minds that will undoubtedly follow us. They will need to answer these questions, plus many other hard questions we can't even predict yet. Nonetheless, we can provide them with the tools they'll need to find the answers.

We and our colleagues across the industry are heirs to Alan Turing and John Von Neumann, the fathers of the classical computer. Without their foundational research, we wouldn't be here today, exploring how to push computing beyond its current limits. Similarly, we aspire to become the pioneers of a new computing paradigm by being the first to build a truly useful quantum computer, the basis upon which generations of other innovators will build.

We're doing this even though no one yet knows the limits of this novel technology. All we know is that a quantum computer will unlock a whole new world of possibilities, both known and unknown.

Together, we have a grand journey ahead; where would you like to go? ■



ALICE & BOB

CONTACT

niccolo.coppola@alice-bob.com

WRITTEN BY

Niccolò Coppola, Raphaël Lescanne, Laurent Prost, Matija Žesko

CURATED BY

Brian Siegelwax

ILLUSTRATED BY

Guillaume Gennet

AUDIO VERSION NARRATED BY

Christopher Bishop

Listen to “Think Inside The Box” on:

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